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ORIGINAL ARTICLE

Identification of current transport mechanism in Al_2O_3 thin films for memory applications

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Abstract The effect of oxygen anneal on the electrical characteristics, especially on the current transport mechanism, of Al_2O_3 films in the thickness range of 10–30 nm was examined in detail. The analyses were performed at electric fields of $\leq$2.5 MV/cm to effectively address the reliability of Al_2O_3-based devices operating in the low electric field regime. The general conduction mechanism equations were used to simulate the expected current density (J) values for a given electric field (E) range. The characteristic linear plots of the conduction mechanisms were then used to compare the experimental and simulated data to identify the most probable mechanism occurring in the dielectric. Parameters like barrier height and activation energy were extracted from the fit. It was found that oxygen anneal has profound effects on the electrical properties of Al_2O_3 films, with annealed films demonstrating a different conduction mechanism than their unannealed counterparts, along with significant improvement in the leakage current and barrier height. This kind of analyses will help optimize the process conditions for Al_2O_3 deposition and provide an optimal range for device operation, thus improving the reliability of Al_2O_3 films for applications in CMOS logic and Flash memory.

Keywords Current transport mechanism · Thin films · Effect of anneal · CMOS logic application

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Introduction

Over the past few decades, the key to the continuous improvement in the performance of the "work horse" of the semiconductor industry, i.e., MOSFET has been scaling (Wilk et al. 2001; He et al. 2011; Robertson 2006). In 1974, when Robert Dennard and his team (Dennard et al. 1974) proposed a set of rules to scale the various device parameters for improved performance, little did they know that it will revolutionize the silicon industry. Throughout this period of extensive scaling, the performance and power specifications of the integrated circuit (IC) were effectively achieved (Robertson 2006), thus allowing the cost per chip to reduce drastically. Hence, the ICs essentially remained a Si-based CMOS technology. However, as scaling continues, (a) SiO_2, used as the gate dielectric, approaches its fundamental limit on physical thickness causing an increase in gate leakage current due to direct tunneling (He et al. 2011, Lee et al. 2006, Kim and Lee 2005), (b) short-channel effects start to dominate (Lee et al. 2006) and (c) current lithographic methods are challenged with the need of light sources with shorter wavelengths (Robertson 2006), thus questioning the device reliability at lower technology nodes and halting any improvement in the device performance. As performance enhancement through geometrical scaling becomes more challenging and demand for higher functionality increases, there is tremendous interest and potential to explore alternative gate stack technology, namely the high-κ dielectrics (Wilk et al. 2001). Over the last decade, traditional SiO_2 has been replaced with SiO_xN_y and then Hf-based high-κ gate dielectrics in an effort to reduce the excessive tunneling leakage current at the gate (Robertson 2006, Lee et al. 2006, Kim and Lee 2005). Some of the critical requirements of a gate dielectric include (Wilk et al. 2001, He

et al. 2011, Robertson 2006, Jones et al. 2005), (a) thermal stability to withstand the high-temperature CMOS process flow, (b) high-quality silicon–insulator interface, (c) high band offset with Si to reduce carrier injection, d) high 'κ' value to support future scaling of the gate dielectric and (e) low gate leakage.

Hf-based dielectrics, HfO_2 for example, has been chosen to replace SiO_2 due to its high 'κ' value (25) and good thermal stability with Si (Lee et al. 2006). However, HfO_2 has a lower bandgap (5.8 eV) compared to SiO_2 (9 eV) and also crystallizes at a lower temperature (Robertson 2006, Bouazra et al. 2008) aiding leakage currents. Reducing the leakage current without degrading the carrier mobility is yet another challenge. It is reported (Lee et al. 2006) that mobility can be enhanced by thinning of the gate dielectric, in turn resulting in increased gate leakage.

Another important application of high-κ dielectric is its use as an inter-poly dielectric (IPD), a.k.a blocking dielectric, in flash memory technology to improve the capacitive coupling for higher performance and reduce the gate leakage for better memory retention and low power dissipation (Kim and Lee 2005). As the name suggests, the blocking dielectric is used to block the leakage of the stored charge from the floating gate of a flash memory. Use of high-κ dielectrics (hence, larger physical thickness) as blocking dielectric can effectively reduce the charge leakage and withstand higher operating voltages, thereby enhancing the programming and erasing speeds of the flash memory. Integration of non-volatile memory (NVM) within CMOS requires cell area scaling and voltage scaling, which is performed by scaling the inter-poly dielectric (IPD) (Wellekens et al. 2007). Since the traditional SiO_2 has reached its physical limit, high-κ dielectrics are the next best thing to be used as IPD. The ITRS 2011 roadmap includes high-κ dielectrics as part of the Flash Memory Technology Requirements, to be used as an IPD, for the coming decade (International Technology Roadmap for Semiconductors 2011).

Among the available high-κ materials, Al_2O_3 is considered to be one of the most suitable candidates for high-performance memory, embedded flash and DRAM applications (Wilk et al. 2001; Lee et al. 2006; Kim and Lee 2005; Wellekens et al. 2008). It has been suggested in literature (Kolodzey et al. 2000) that sputterred Al_2O_3 has an increased capacitive coupling and performance compared to conventional SiO_2. Al_2O_3 is found to be immune to erase saturation and its memory retention capability is superior to that of HfO_2 (Wellekens et al. 2007). It is chemically and thermodynamically stable and forms an atomically abrupt interface with Si (Afanas'Ev et al. 2002), making it a suitable replacement for SiO_2. Al_2O_3 has a large band gap ($\approx$8.7 eV) (Robertson 2006; Kolodzey et al. 2000) and higher crystallization temperature compared to HfO_2 (Robertson 2006; Bouazra et al. 2008) and proven electrical characteristics. Hence, it is rightly being pursued for use as blocking dielectric in flash memories (Dutta et al. 2011). Fig. 1 shows a schematic of a gate stack structure used in flash memory.

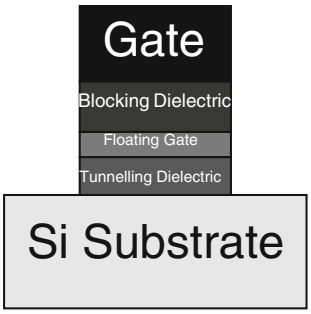

Fig. 1 Schematic of flash memory gate stack structure

The study of current transport mechanism of the gate dielectric provides valuable insight into the reliability characteristics of the devices (Kim and Lee 2005; Bouazra et al. 2008; Lee et al. 2004). Hence, a proper understanding of the mechanisms in the high-κ dielectrics for flash memory and CMOS logic applications is necessary for a better design.

In this paper, we report the current transport mechanisms observed in Al_2O_3 thin films in the thickness range 10–30 nm. It has been reported in literature (Wellekens et al. 2008) that increased retention in NVM is achieved using a thicker Al_2O_3 IPD. So understanding the current transport mechanism in this thickness range is critical. We also analyze the effect of oxygen anneal on the current transport mechanisms and the electrical characteristics of Al_2O_3 thin films in the electric field regime $\leq$2.5 MV/cm to effectively address the reliability concerns of Al_2O_3-based devices, operating under low electric fields, specifically for CMOS logic and flash memory applications.

Experiments

The MOS capacitors used for analysis were fabricated on p-Si (100) substrates with a resistivity of 0.01–0.02 Ω cm. After RCA clean, thin Al_2O_3 films were deposited by physical vapor deposition with an oxygen flow rate of 25 sccm and with target powers of 500 and 1000 W, at room temperature. Thickness and refractive index of the films were measured by Spectroscopic Ellipsometer (SE 800). This was followed by a post-deposition anneal (PDA) on selected samples. Finally after an aluminium gate metallization of all the samples, the devices were ready for electrical characterization. The unannealed Al_2O_3 samples were fabricated to study the effect of anneal in the current

Table 1 Process data for samples fabricated with different thicknesses and annealing conditions

Sample	Thickness (nm)	Refractive index	Annealing condition
Sample 1	12.7	1.65	15 s, 1000 °C in O_2
Sample 2_a	27	1.6	Unannealed
Sample 2_b	24	1.7	15 s, 1000 °C in O_2

transport mechanism. The PDA was carried out in oxygen ambient at 1000 °C for 15 s. A high PDA temperature is desired as it improves the program/erase performance (Wellekens et al. 2008).

The I–V characteristics were measured using Keithley 4200 SCS fully shielded probe station with triax chuck. The high-temperature I–V characteristics were measured for the samples in the voltage range 0–3 V. The measurements were conducted at different temperatures −25, 50, 100, 150 and 200 °C. Table 1 summarizes the process conditions of the Al_2O_3 samples that were used for analysis.

Results and discussions

The current-voltage (I–V) characteristics of a dielectric can be influenced by different conduction mechanisms each dominating in a certain temperature and voltage range. Some of the possible mechanisms that can occur in a dielectric include Schottky emission, Frenkel–Poole emission, Fowler-Nordheim, Space Charge Limited and Ohmic conduction (Sze 2010).

Table 2 summarizes the different possible relation between current density (J) and the electric field (E). The relations govern the conduction mechanism in a dielectric. The table also gives the characteristic linear plots for each mechanism. These conduction mechanism equations were used to simulate the expected 'J' values for a given 'E' range. Table 3 gives the values of constants used in simulation. The characteristic linear plots were then used to compare the experimental and simulated data to identify the most probable mechanism occurring in the dielectric. Certain dielectric parameters like Schottky barrier height, space charge power number were extracted from the fit and discussed.

Table 2 Basic current transport mechanisms (Jones et al. 2005; Sze 2010; Perera et al. 2003; Chiu 2006)

Mechanism	J–V relation	Linear plot
Schottky emission	$J = A^* T^2 \exp\left\{-q\frac{\phi_B - \sqrt{\frac{qE}{4\pi\epsilon_0\epsilon_d}}}{k_B T}\right\}$	$ln(J/T^2)$ vs. $\sqrt{E}$
Frenkel–Poole emission	$J = E \exp\left\{-q\frac{\phi_t - \sqrt{\frac{qE}{\pi\epsilon_0\epsilon_d}}}{k_B T}\right\}$	$ln(J/E)$ vs. $\sqrt{E}$
Fowler–Nordheim emission	$J = E^2 \exp\left\{\frac{-8\pi\sqrt{2qm^*}\phi_B^3}{3hE}\right\}$	$ln(J/E^2)$ vs. $(1/E)$
Space charge limited emission	$J \propto E^n$	$ln(J)$ vs. $\ln(E)$
Ohmic conduction	$J \approx E \exp\left(\frac{-\Delta E_{ae}}{k_B T}\right)$	J vs. E

Table 3 Constants used in Simulation (Jones et al. 2005; Bouazra et al. 2008; Lu et al. 2006)

Parameter	Value
Boltzmann constant (k_B)	1.38×10^{-23} J/K
Electron charge (q)	1.602×10^{-19} C
Permittivity of free space (ϵ_0)	8.854×10^{-14} F/cm
Dielectric refractive index (n)	1.65
Dynamic permittivity (ϵ_d)	n^2
Free electron mass (m_0)	9.1×10^{-31} Kg
Effective electron mass of dielectric (m^*)	$0.35 \times m_0$
Richardson constant (A^*)	$120[\frac{m^*}{m_0}]$
Barrier height (ϕ_B)	To be extracted from fit
Electron activation energy (ΔE_{ae})	To be extracted from fit

Sample 1

The J vs. E plots of the MOS capacitors from sample 1, measured at different temperatures, are shown in Fig. 2. The plots show three regions (≤1 MV/cm, 1–1.7 MV/cm and 1.7–2.4 MV/cm) of dependence of the current density on the applied electric field. This is due to different conduction mechanisms governing each of those regions. The equations of some of the commonly occurring conduction mechanisms were used to simulate a fit and analyze the experimental data in each of the three regions.

1. Conduction in region 1 (≤1 MV/cm): Figs. 3, 4 show the comparison of the experimental data with Frenkel–Poole and Ohmic conduction mechanisms. We can see that the experimental and simulated data do not fit. At electric fields ≤1 MV/cm the experimental data match best with the Schottky emission. Fig. 5 shows the comparison of the characteristic Schottky plots of both experimental and simulated data at two different temperatures. It has been reported (Cimpoiasu et al. 2004) that for a dielectric at room temperature, a barrier height of ≥1.5 eV is sufficient to suppress the thermionic current, in turn reducing the leakage. The Schottky barrier height, ϕ_B obtained from the above fit is 1.35 ± 0.25 eV, which is close to the desired value. Also interesting to note is that this value is higher compared to the value (0.78 eV) reported for Al_2O_3 in literature for a thickness range for 100 nm

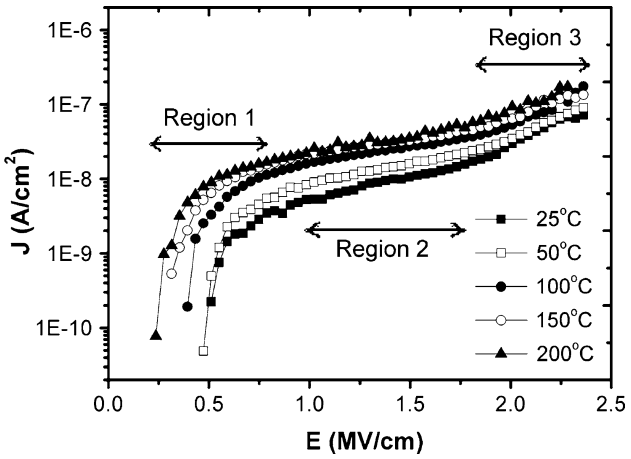

Fig. 2 J vs. E characteristics of sample 1 measured at different temperatures

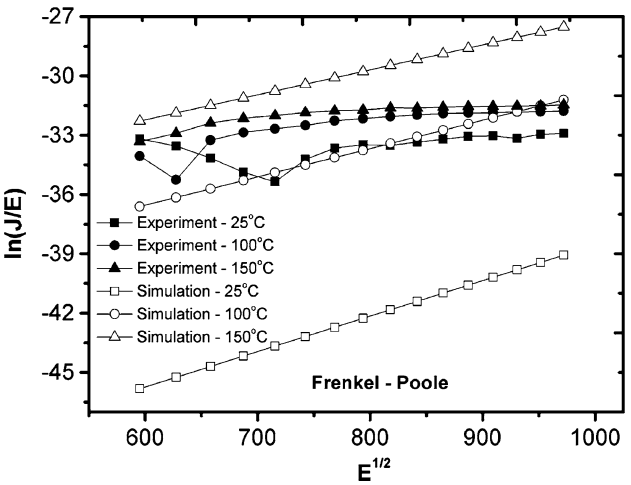

Fig. 3 Comparison of experimental data with possible conduction mechanisms in region 1 of sample 1. The mismatch for Frenkel–Poole with measured data is shown

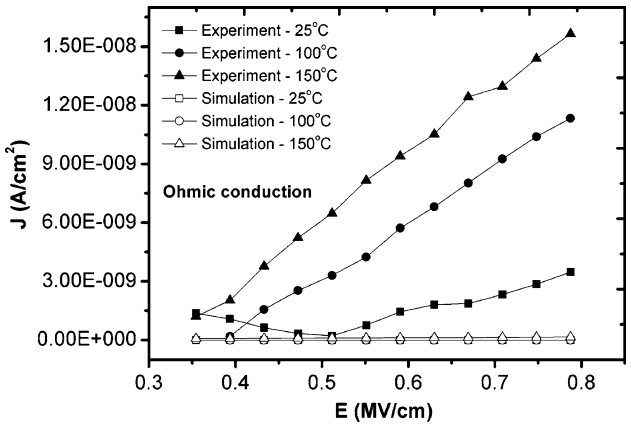

Fig. 4 Comparison of experimental data with possible conduction mechanisms in region 1 of sample 1. The mismatch for Ohmic conduction with measured data is shown

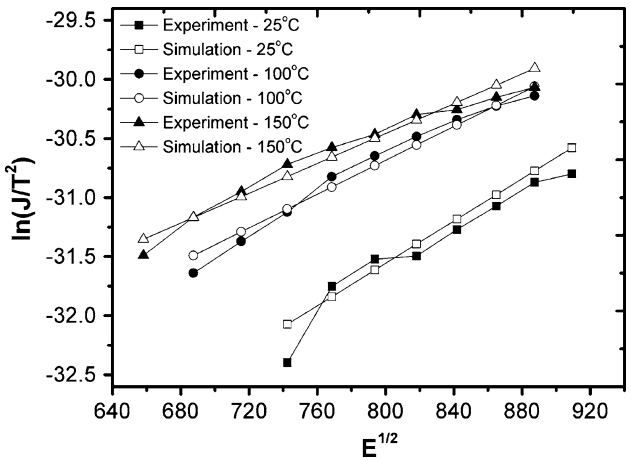

Fig. 5 The $ln(J/T^2)$ vs. $\sqrt{E}$ linear Schottky plots at different temperatures at electric fields $\leq$1 MV/cm. Also shown are the simulated fits for the data in this region

(Mikhaelashvili et al. 1998). It is most possible that the PDA at a high temperature has increased the bandgap and band offsets of Al_2O_3, resulting in an increase in barrier height, thus reducing the leakage current (Wellekens et al. 2007; Cimpoiasu et al. 2004).

2. Conduction in region 2 (1–1.7 MV/cm): In this region, the current density of the device seemed to satisfy a power law relation with the electric field, given by,

$$J \propto E^n \quad (1)$$

The above relation suggests the presence of the Space charge limited mechanism. The power number, n can be calculated from the slope of this plot. In general, $n \approx 3$ for dielectrics with traps (Perera et al. 2003). However, the average power number obtained from the simulated fit of experiment data is $n = 1.41$. A lower power number indicates a reduction in the space charge current in this region. This reduction can be attributed to the injection of charge carriers at the gate electrode–dielectric interface (Perera et al. 2003). This mechanism can degrade data retention and must be carefully addressed. Fig. 6 shows the Space charge fit for the measured data in region 2. Figs. 7 and 8 show the mismatch of experimental data with Frenkel–Poole and Ohmic conduction mechanisms in this region.

3. Conduction in region 3 (1.7–2.4 MV/cm): The Frenkel–Poole and Schottky mechanisms do not match with the experimental data (see Figs. 9 10). In this region, the experiment data fit best with the Ohmic conduction mechanism. The electron activation energy obtained from the fit is 0.98 ± 0.2 eV. Figure 11 shows the fit for experiment data at two different temperatures in region 3. The tail observed in the plot is presumably the transition from and/or to another mechanism.

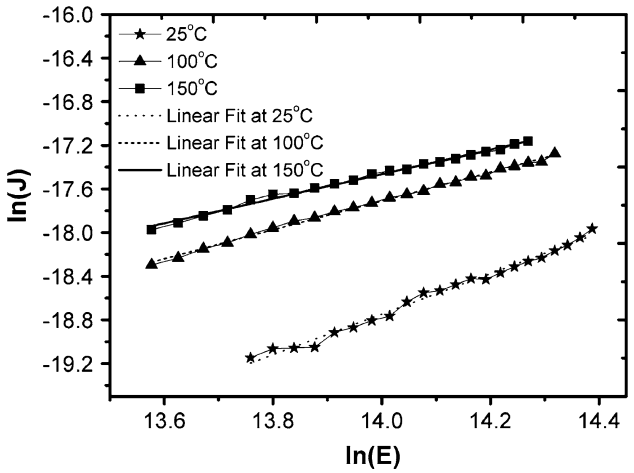

Fig. 6 Space charge plots [$ln(J)$ vs. $ln(E)$] of measured data and the corresponding linear fits in the region 1–1.7 MV/cm

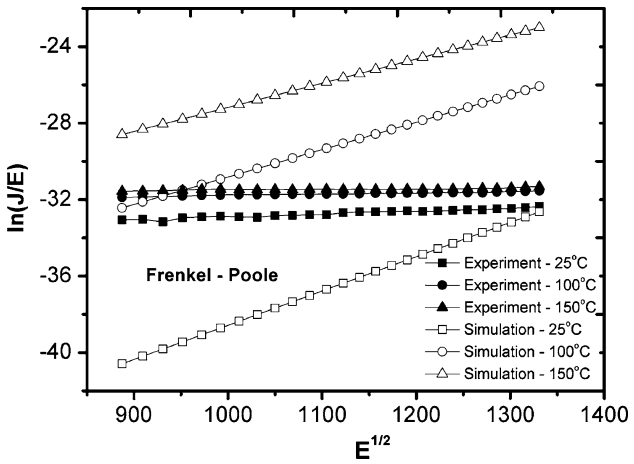

Fig. 7 The mismatch of experimental data with Frenkel–Poole mechanism in region 2 of sample 1

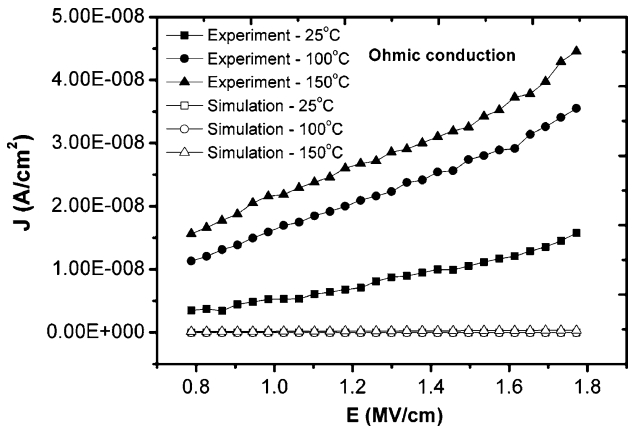

Fig. 8 The mismatch of experimental data with Ohmic conduction mechanism in region 2 of sample 1

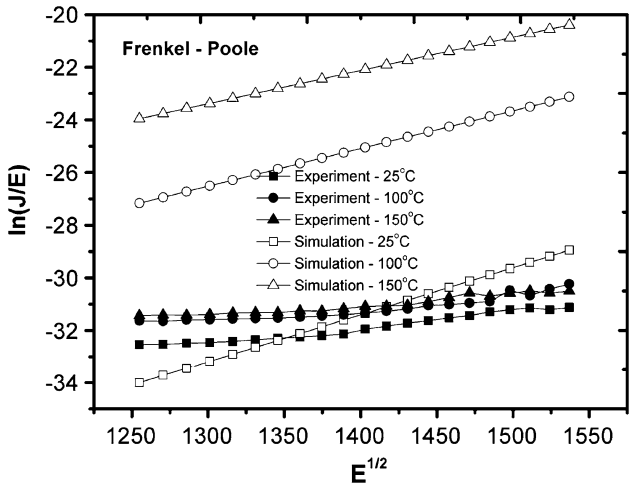

Fig. 9 Comparison of experimental data with possible conduction mechanisms in region 3 of sample 1. The mismatch for Frenkel–Poole with measured data is shown

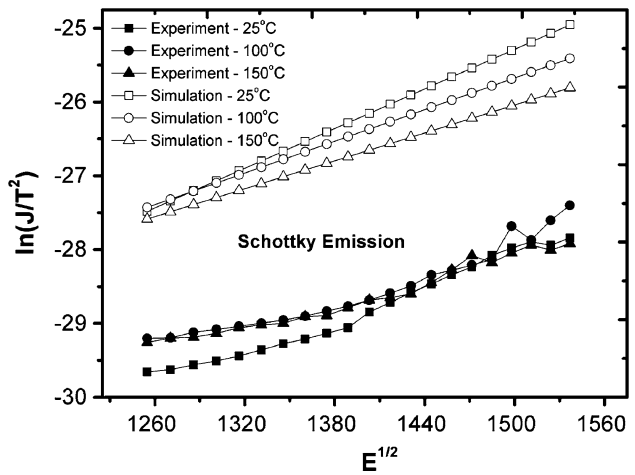

Fig. 10 Comparison of experimental data with possible conduction mechanisms in region 3 of sample 1. The mismatch for Schottky emission with measured data is shown

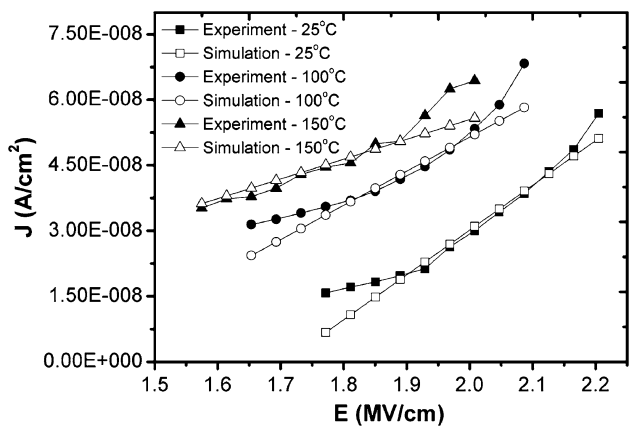

Fig. 11 The J vs. E linear Ohmic plots in the region 1.7–2.4 MV/cm. Simulated ohmic plots fit best in this region

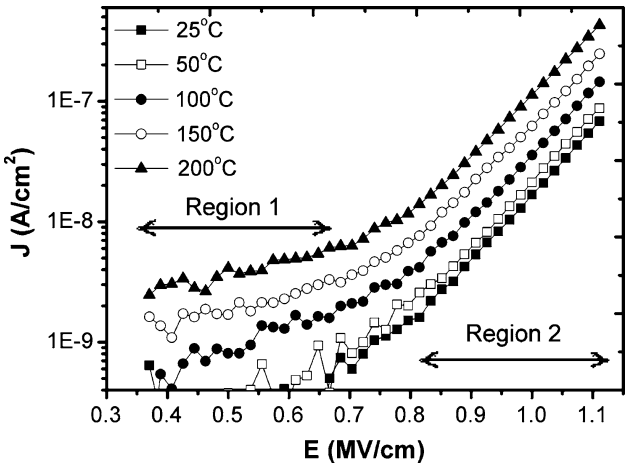

Fig. 12 J vs. E characteristics of sample 2_a at different temperatures

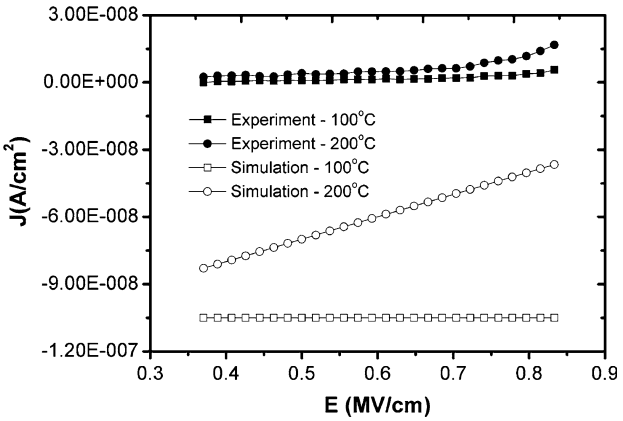

Fig. 14 Comparison of the experimental data with possible mechanisms in sample 2_a. The mismatch for Ohmic conduction with measured data is shown

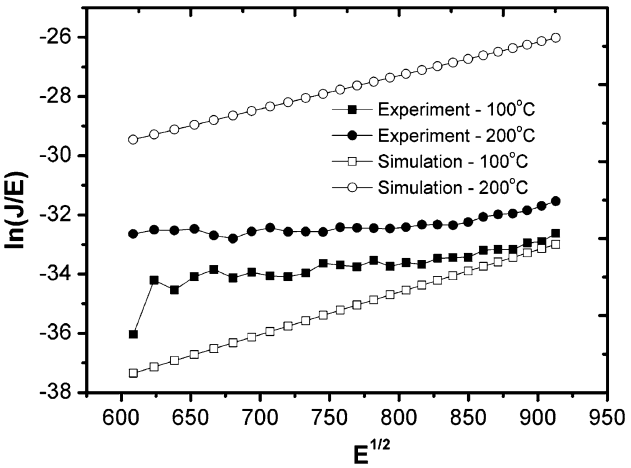

Fig. 13 Comparison of the experimental data with possible mechanisms in sample 2_a. The mismatch for Frenkel–Poole with measured data is shown

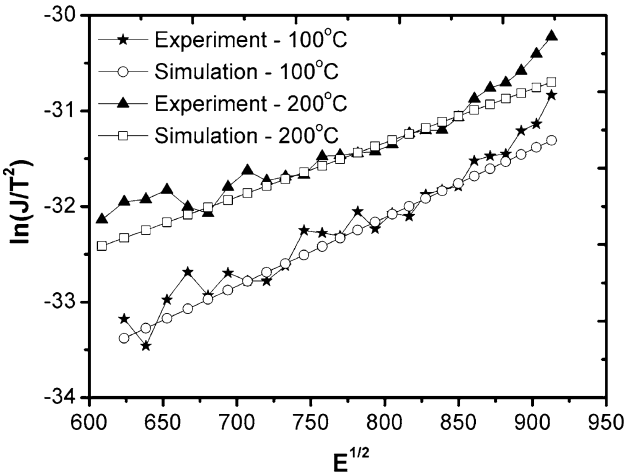

Fig. 15 The $ln(J/T^2)$ vs. $\sqrt{E}$ plots of experiment and simulated data at different temperatures in the electric field region $\leq$0.8 MV/cm

Sample 2_a

Sample 2_a is an unannealed sample (see Table 1). The J vs. E plots of the sample, measured at different temperatures, are shown in Fig. 12. The plots show two regions ($\leq$0.8 MV/cm and 0.8–1.1 MV/cm) of dependence of the current density on the applied electric field. The Frenkel–Poole mechanism and the Ohmic conduction do not match with the data in the entire region of analysis from 0 to 1.1 MV/cm (see Figs. 13, 14).

The experimental data fit with the Schottky emission in the region $\leq$0.8 MV/cm. Fig. 15 shows the experiment and simulated Schottky plots. However, for the region 0.8–1.1 MV/cm, there are no fit available. So it is most likely that multiple mechanisms are at play, though the reason is unknown at this point.

Sample 2_b

The J vs. E plots of the annealed sample, measured at different temperatures, are shown in Fig. 16. Interestingly, we can see a single region (0.4–1.7 MV/cm) of discernible dependence of the current density on the applied electric field. It is possible that a single type of current transport mechanism is dominating in this sample through out the applied voltage range. Also, the current density of the annealed sample 2_b is an order of magnitude less compared to the unannealed sample 2_a.

Initially when Al_2O_3 film is deposited at room temperature, it is in amorphous state. A thermal anneal leads to a gradual ordering and densification of the film (Afanas'Ev et al. 2002; Cimpoiasu et al. 2004). Thus, the oxygen anneal resulted in lesser number of defects or traps,

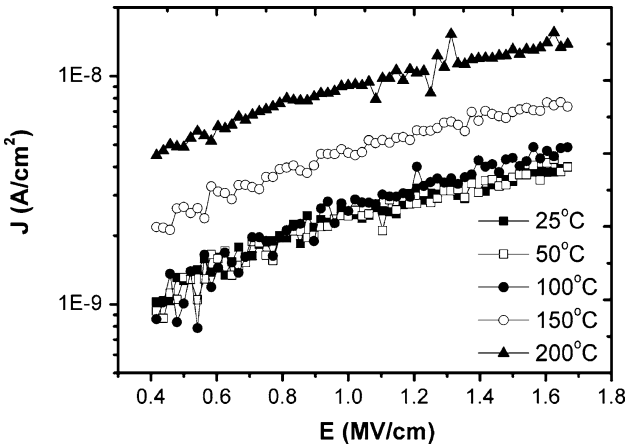

Fig. 16 J vs. E characteristics of sample 2_b at different temperatures

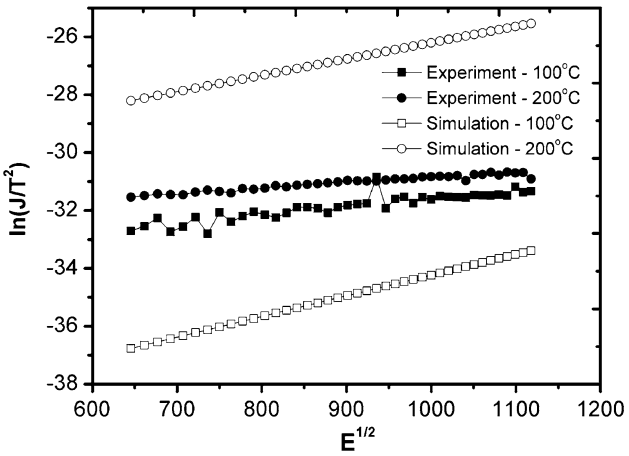

Fig. 18 Comparison of the experimental data with possible mechanisms in sample 2_b. The mismatch for Schottky emission with measured data is shown

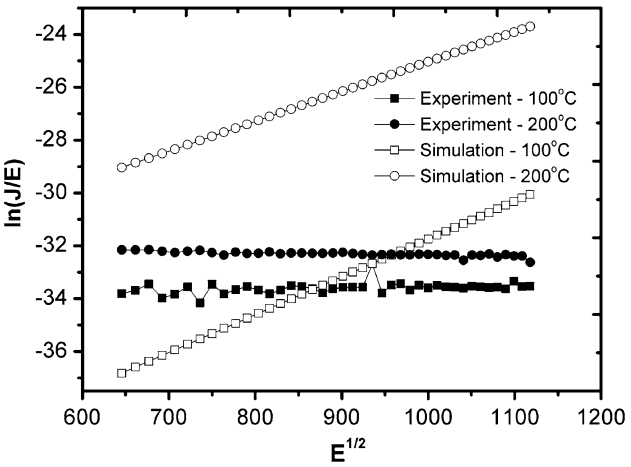

Fig. 17 Comparison of the experimental data with possible mechanisms in sample 2_b. The mismatch for Frenkel–Poole with measured data is shown

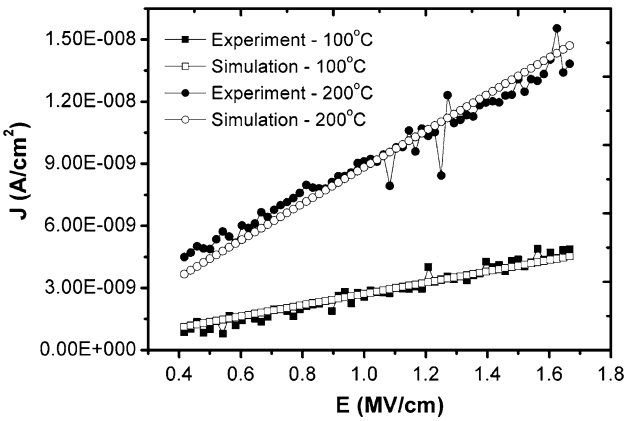

Fig. 19 Ohmic plots of experiment and simulated data in the region 0.4–1.7 MV/cm

reducing the leakage current (Aguado et al. 2007; Paskaleva et al. 2002).

Since the electric field is very low (≤2 MV/cm) and the films are thick enough (24 nm), possibility of electrons tunneling through the dielectric is very less. Figs. 17 and 18 show the comparison of the data with Frenkel–Poole and Schottky mechanisms. Further analysis revealed that the conduction mechanism in the annealed sample matched with both Ohmic conduction and Space Charge Limited. However, the Space charge power number obtained from fit is close to unity or in other words $J \propto E$ which is similar to the Ohmic conduction relation from Table 2 ($J \approx E\exp(\frac{-\Delta E_{ae}}{k_B T})$). So we can safely conclude that Ohmic conduction is the dominant mechanism in this sample. There is a plausible explanation to this assumption. Current conduction in the ohmic mechanism is governed by a hopping mechanism, where the electrons hop between the defect states present in the dielectric (Perera et al. 2003). These defect states could be due to the formation of mobile interstitial Si species (Dutta et al. 2011). During the anneal, O_2 diffuses into the dielectric and reacts with the bulk Si at the dielectric–substrate interface. The oxidized Si, then occupies a larger volume, thus, generating mobile interstitial Si species. It is reasonable to conclude that the O_2 anneal has changed the dominant conduction mechanism from multiple in unannealed sample to a dominant ohmic conduction in the annealed sample. This way, by carefully changing the process conditions, the type of conduction mechanism occurring in the dielectric can be effectively controlled. Fig. 19 shows the Ohmic conduction fit with measured data. The electron activation energy was found to be 1.08 eV from the fit.

Table 4 Analysis summary

Sample	Region of analysis	Mechanism observed and remark
Sample 1	≤1 MV/cm	Schottky emission: improvement in ϕ_B due to high-temperature PDA; possible reduction in leakage current
Sample 1	1–1.7 MV/cm	Space charge limited: lower power number due to carrier injection at the electrode; can degrade memory retention
Sample 1	1.7–2.4 MV/cm	Ohmic conduction
Sample 2_a	≤1.1 MV/cm	Multiple mechanisms playing a role; not desired; difficult to predict the electrical characteristics in this operating region
Sample 2_b	0.4–1.7 MV/cm	Ohmic conduction: formation of mobile Si species due to PDA; transformation of conduction mechanism after anneal; process conditions can be carefully altered to control the mechanism occurring in the dielectric

Conclusions

MOS capacitors with PVD Al_2O_3 as dielectric were fabricated. The effect of O_2 anneal on the current transport mechanism of Al_2O_3 was studied. Table 4 lists out the conduction mechanisms observed under different operating fields for each sample. The table also summarizes the inference made from the analysis. It is observed that annealing in O_2 improves the barrier height at the gate electrode–dielectric interface, thus reducing the leakage current. Reduction in current conduction can improve the reliability of devices operating under extreme conditions. Multiple mechanisms play a role in the unannealed sample, which makes the prediction of electrical characteristics and reliability very difficult. We also found that the high-temperature O_2 anneal has completely transformed the conduction mechanism of the dielectric. The above analysis of current transport mechanisms in different regions of operating fields for Al_2O_3 will give a broad insight and help choose the appropriate voltage range for operation for Al_2O_3-based memory devices. The role of process conditions in modifying the conduction mechanism occurring in the dielectric is more clear and these observations will help improve the process conditions for Al_2O_3 and its reliability for CMOS logic and Flash memory applications.

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References

Afanas'Ev VV, Stesmans A, Mrstik BJ, Zhao C (2002) Impact of annealing-induced compaction on electronic properties of atomic-layer-deposited Al_2O_3. Appl Phys Lett 81(9):1678–1680

Aguado DR, Govoreanu B, Degraeve R, Van Houdt J, De Meyer K (2007) A Study of the as-processed and generated leakage paths in Al_2O_3-based dielectric stacks for nonvolatile memory applications. ESSDERC 2006 - Proceedings of the 36th European Solid-State Device Research Conference, art. no. 4099942:407–410

Bouazra A, Abdi-Ben Nasrallah S, Poncet A, Said M (2008) Current tunnelling in MOS devices with Al_2O_3/SiO_2 Gate Dielectric. Res Lett Phys. doi:10.1155/2008/286546

Chiu FC (2006) Interface characterization and carrier transportation in metal/HfO_2/silicon structure. J Appl Phys 100(11): 114102

Cimpoiasu E, Tolpygo SK, Liu X, Simonian N, Lukens JE.Likharev KK, Klie RF, Zhu Y (2004) Aluminum oxide layers as possible components for layered tunnel barriers. J Appl Phys 96(2):1088–1093

Dennard RH, Gaensslen FH, Yu H-N, Rideout VL, Bassous E, LeBlanc AR (1974) Design of Ion-Implanted MOSFET's with very small physical dimensions. IEEE J Solid-State Circuits, SC-9(5):256–268

Dutta S, Ramesh S, Shankar B, Gopalan S (2011) Effect of PVD process parameters on the quality and reliability of thin (10–30 nm) Al_2O_3 dielectrics. Appl Nanosci. doi:10.1007/s13204-011-0033-0

He G, Zhu L, Sun Z, Wan Q, Zhang L (2011) Integrations and challenges of novel high-k gate stacks in advanced CMOS technology. Prog Mater Sci 56(5):475–572

International Technology Roadmap for Semiconductors (2011) Process integration, devices and structures, 2011 ITRS Edition

Jones MN, Kwon YW, Norton DP (2005) Dielectric constant and current transport for HfO_2 thin films on ITO. Appl Phys A Mater Sci Process 81(2):285–288

Kim YH, Lee JC (2005) Hf-based high-κ dielectrics: process development, performance characterization, and reliability. Morgan and Claypool Publishers, USA, ISBN 1598290045

Kolodzey J, Chowdhury EA, Adam TN, Qui G, Rau I, Olowolafe JO, Suehle JS, Chen Y (2000) Electrical conduction and dielectric breakdown in aluminum oxide insulators on silicon. IEEE Trans Electron Devices 47(1):121–128

Lee JH, Kim JP, Lee JH, Kim YS, Lim HJ, Jung HS, Doh SJ, Lee NI, Kang HK (2004) Lifetime projections and conduction mechanisms for Hafnium based high-κ capacitor dielectrics using low thermal budget process. Annual Proceedings — Reliability Physics (Symposium), 579–580

Lee BH, Oh J, Tseng HH, Jammy R, Huff H (2006) Gate stack technology for nanoscale devices. Mater Today 9(6):32–40

Lu YK, Chen XF, Zhu W, Gopalkrishnan R (2006) Growth and characterization of HfO_2 high-κ gate dielectric films by laser molecular beam epitaxy (LMBE). J Mater Sci 17(9):685–688

Mikhaelashvili V, Betzer Y, Prudnikov I, Orenstein M, Ritter D, Eisenstein G (1998) Electrical characteristics of metal-dielectric-metal and metal-dielectric-semiconductor structures based on electron beam evaporated Y_2O_3, Ta_2O_5 and Al_2O_3 thin film. J Appl Phys 84(12):6747–6752

Paskaleva A, Atanassova E, Novkovski N, Pecovska-Gjorgjevich M (2002) Conduction mechanisms in thin RF sputtered Ta_2O_5 films on Si and their dependence on O_2 annealing. MIEL 2002 - 23rd International Conference on Microelectronics, 2, pp. 755–758

Perera R, Ikeda A, Hattori R, Kuroki Y (2003) Trap assisted leakage current conduction in thin silicon oxynitride films grown by rapid thermal oxidation combined microwave excited plasma nitridation. Microelectronic Eng 65(4):357–370

Robertson J (2006) High dielectric constant gate oxides for metal oxide Si transistors. Rep Prog Phys 69(2):327–396

Sze SM, Ng Kwok K (2010) Physics of semiconductor devices, 3rd edn, Wiley, New Delhi, India

Wellekens D, Blomme P, Govoreanu B, De Vos J, Haspeslagh L, Van Houdt J, Brunco DP, Van Der Zanden K (2007) Al_2O_3 Based flash interpoly dielectrics: a comparative retention study. ESSDERC 2006-Proceedings of the 36th European Solid-State Device Research Conference, art. no. 4099900, 238–241

Wellekens D, De Vos J, Van Houdt J, Van Der Zanden K (2008) Optimization of Al_2O_3 Interpoly Dielectric for Embedded Flash Memory Applications. Joint Non-Volatile Semiconductor Memory Workshop and International Conference on Memory Technology and Design, Proceedings, NVSMW/ICMTD, art. no. 4531809, 12–15

Wilk GD, Wallace RM, Anthony JM (2001) High-κ gate dielectrics: current status and materials properties considerations. J Appl Phys 89(10):5243–5275

Yang BL, Lai PT, Wong H (2004) Conduction mechanisms in MOS gate dielectric films. Microelectronics Reliability 44(5):709–718